CLAIMS

1. A semiconductor device comprising:

an electrode;

a top region of a second conductivity type connected to the electrode;

a deep region of the second conductivity type;

an intermediate region of a first conductivity type connected to the electrode, the intermediate region isolating the top region and the deep region;

a gate electrode facing a portion of the intermediate region via an insulating layer, the portion of the intermediate region isolating the top region and the deep region; and

a barrier region formed within the intermediate region and/or the top region.

2. A semiconductor device according to claim 1,

wherein the intermediate region comprises a dense portion directly connected to the electrode, and a main portion connected to the electrode via the dense portion.

3. A semiconductor device according to claim 2,

wherein the top region is an emitter, the dense portion is a body contact, the main portion is a body, the deep region is a drift, and the semiconductor device is an IGBT.

4. A semiconductor device according to any one of the preceding claims,

wherein the barrier region comprises a semiconductor region of the second conductivity type, this being electrically disconnected from the electrode and the deep region.

5. A semiconductor device according to claim 4,

wherein the barrier region is connected to the insulating layer, and the barrier region has an opening through which carriers may flow between the dense portion and the deep region.

6. A semiconductor device according to any one of the preceding claims, wherein the barrier region comprises an insulator.

7. A semiconductor device according to any one of the preceding claims, wherein the barrier region comprises a semiconductor region of the first conductivity type having a higher concentration of impurities than the main portion, the semiconductor region having the higher concentration of impurities being formed along a boundary between the top region and the main portion and being electrically connected to the dense portion.

8. A semiconductor device according to any one of claims 2 to 7, wherein the barrier region is formed in the vicinity of a boundary between the dense portion and the main portion,

the semiconductor device further comprising an additional barrier region of the second conductivity type formed in the vicinity of a boundary between the main portion and the deep region, the additional barrier region being electrically disconnected from the electrode and the deep region.

9. A semiconductor device according to any one of claims 2 to 8, wherein the barrier region is formed in the vicinity of a boundary between the dense portion and the main portion,

the semiconductor device further comprising an additional barrier region of the second conductivity type formed in the vicinity of a boundary between the main portion and the deep region, the additional barrier region having a higher concentration of impurities than the deep region.

10. A semiconductor device according to claim 8 or 9,

wherein at least a portion of the barrier region and a portion of the additional barrier region are located on a path along which carriers flow.

11. A semiconductor device according to any one of the preceding claims,

wherein a plurality of barrier regions is formed within the intermediate region, the barrier regions being distributed within the intermediate region.

12. A semiconductor device according to claim 11,

wherein a plurality of pairs of barrier layer and intermediate layer is stacked.

13. A semiconductor device according to any one of the preceding claims,

wherein the barrier region is connected to the dense portion.

14. A semiconductor device according to any one of the preceding claims,

wherein the thickness of the top region is less than the thickness of the barrier region.